Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1–7 (previously canceled)

Claim 8 (currently amended). ~~An Ethernet switch including a plurality of ports (n), each port comprising:~~

~~an ingress/egress port;~~

An ingress/egress port for an Ethernet switch comprising:

a plurality of Media Access Control (MAC) interfaces, each MAC interface is capable of receiving/transmitting Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configurable to receive/transmit Gigabit Ethernet (GE) packets;

receive and transmit modules which are configurable respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces; and

wherein the ingress/egress port is switchable between a first mode and a second mode, in which the ingress/egress port operates as a single GE port in the first mode and as more than one FE port in the second mode.

~~wherein at least a portion of the plurality of ports are switchable between two modes in which the portion of the plurality of ports operate respectively as one GE port or a plurality of FE ports (m), and wherein there are m MAC interfaces per port, wherein the switch is configured to operate as n GE ports and m (m-n) FE ports where n is a selectable integer greater than 1 and m is an integer greater than 1.~~

Claim 9 (currently amended). The ingress/egress port ~~switch~~ according to claim 8 wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, the other MAC interfaces only being adapted to receive/transmit FE packets.

Claim 10 (currently amended). The ingress/egress port ~~switch~~ according to claim 9 wherein which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

Claim 11 (currently amended). The ingress/egress port ~~switch~~ according to claim 8 wherein which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

Claim 12 (currently amended). The ingress/egress port ~~switch~~ according to claim 8 wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

Claim 13 (currently amended). The ingress/egress port ~~switch~~ according to claim 12, wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces, and wherein the receiver interface is further operable to fetch packet data from the set of buffers and store the packet data in the memory.

Claim 14 (currently amended). The ingress/egress port ~~switch~~ according to claim 13, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

Claim 15 (currently amended). The ingress/egress port ~~switch~~ according to claim 13, wherein the receiver interface is further operable to store the descriptor associated with the packet data in the memory.

Claim 16 (currently amended). The ingress/egress port ~~A switch~~ according to claim 8 wherein the plurality of MAC interfaces consists of 8 MAC interfaces.

Claim 17 (currently amended). An Ethernet switch comprising:

~~a plurality of ports (n), each port including~~

~~an~~at least one ingress/egress port, each ingress/egress port having~~,~~

a plurality of Media Access Control (MAC) interfaces, each MAC interface capable of receiving/transmitting Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configurable to receive/transmit Gigabit Ethernet (GE) packets,

receive and transmit modules which are configurable respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces; and

wherein each ingress/egress port is switchable between a first mode and a second mode, in which each ingress/egress port operates as a single GE port in the first mode and as more than one FE port in the second mode.

~~wherein at least a portion of the plurality of ports are switchable between a first mode and a second mode, wherein the portion of the plurality of ports operate as a single GE port in the first mode and the portion of the plurality of ports operate as multiple FE ports (m) in the second mode, wherein there are m MAC interfaces per port, and wherein the Ethernet switch can operate as n GE ports and m (m-n) FE ports where n is a selectable integer greater than 1 and m is an integer greater than 1~~

Claim 18 (cancelled)

Claim 19 (currently amended). The Ethernet switch according to claim 17, wherein the ~~plurality of ports~~ at least one ingress/egress port comprises eight ingress/egress ports, each ingress/egress port being switchable between a first mode and a second mode, in which each ingress/egress port operates as a single GE port in the first mode and as eight FE ports in the

second mode and wherein the switch can operate as *n* GE ports and 8(8-*n*) FE ports for *n* a selectable integer in the range 0 and 8.

Claim 20 (previously presented). The Ethernet switch according to claim 17, wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

Claim 21 (previously presented). The Ethernet switch according to claim 20, wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces, and wherein the receiver interface is further operable to fetch packet data from the set of buffers and store the packet data in the memory.

Claim 22 (previously presented). The Ethernet switch according to claim 21, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

Claim 23 (previously presented). The Ethernet switch according to claim 21, wherein the receiver interface is further operable to store the descriptor associated with the packet data in the memory.

Claim 24 (currently amended). A method, comprising

providing data packets to an ingress/egress port of an Ethernet switch, ~~having a plurality of ports (n), each of~~ the ~~plurality of ports having an~~ ingress/egress port ~~and~~ having a plurality of Media Access Control (MAC) interfaces, each ~~of the plurality of~~ MAC interface[[s]] capable of receiving/transmitting Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configurable to receive/transmit Gigabit Ethernet (GE) packets; ~~and~~

passing packet data from the data packets to ~~one or more~~ a receive module[[s]], the ~~one or more~~ receive module[[s]] configurable to receive both GE and FE packets from all the MAC interfaces;

passing outgoing packet data from ~~one or more~~ a transmit module[[s]] to the MAC interfaces, the ~~one or more~~ transmit module[[s]] configurable to transmit both GE and FE packets to all the MAC interfaces; and

switching the ingress/egress port between a first mode and a second mode, in which the ingress/egress port operates as a single GE port in the first mode and as more than one FE port in the second mode.

~~switching at least a portion of the plurality of ports between two modes, wherein the portion of the plurality of ports operate as one GE port in a first mode and a plurality of FE ports (m) in a second mode, wherein there are m MAC interfaces per port, and wherein the switch is configured to operate as n GE ports and m (m-n) FE ports where n is a selectable integer greater than 1 and m is an integer greater than 1.~~

Claim 25 (previously presented). The method according to claim 24, further comprising providing a control signal to determine whether the MAC interfaces operate as FE interfaces or whether the at least one interface operates as a GE interface.

Claim 26 (previously presented). The method according to claim 25, wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, and the other MAC interfaces are only adapted to receive/transmit FE packets.

Claim 27 (previously presented). The method according to claim 24, wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, and the other MAC interfaces are only adapted to receive/transmit FE packets.

I. Status of the Application

Claims 8 – 17 and 19 – 27 were pending in this application. In this response, applicants have amended claims 8-17, 19 and 24. Support for these amendments can be found in original claims 1 and 6 and in Figure 1. Therefore, claims 8 – 17 and 19 – 27 remain pending.

II. Rejection of Claims 8 – 17 and 19 – 27 Under 35 U.S.C. § 112

In the May 29, 2008 Office action, the examiner rejected claims 8 – 17 and 19 – 27 under 35 U.S.C. § 112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully submit that the examiner's rejection under 35 U.S.C. § 112, second paragraph, is moot in view of the foregoing amendments to claims 8, 17 and 24.

III. Rejection of Claims 8, 17 and 24 Under 35 U.S.C. § 103(a)

In the May 29, 2008 office action, the examiner rejected claims 8, 17, and 24 under 35 U.S.C. § 103(a) as allegedly being obvious over Tzeng et al. (US Publication No. 2003/0212815), hereinafter referred to as "Tzeng", in view of Moran et al. (US Publication No. 2002/0071398), hereinafter referred to as "Moran". In view of the amendment to claims 8, 17 and 24, applicant respectfully submits that the rejection of claims 8, 17 and 24 under 35 U.S.C. § 103(a) is now moot and should be withdrawn.

Applicant respectfully submits that Tzeng and Moran, either alone or in combination, does not teach or suggest the following limitations of claims 8, 17 and 24:

(i) receive and transmit modules which are configurable to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces

(ii) the ingress/egress port is switchable between a first mode and a second mode, in which the ingress/egress port operates as a single GE port in the first mode and as more than one FE port in the second mode

Tzeng, Moran or a valid combination thereof does not disclose, teach or suggest feature (i)

Applicant gratefully acknowledges the Examiner's admission that Tzeng does not disclose separate receive and transmit modules.

Moran discloses a Media Access Controller (MAC 14) interacting with separate receive 30 and transmit 29 storage modules (Figure 2). Clearly, the receive and transmit storage modules in Moran are interacting with only a single MAC interface. Therefore, Moran does not disclose feature (i).

Configuring the receive and transmit modules to interact with all the MAC interfaces not only eliminates the need for additional receive or transmit modules but also allows the full utilization of the bandwidth of the receive and transmit modules in either modes. Such a result is not predictable or expected by Tzeng, Moran or a valid combination thereof.

Tzeng, Moran or a valid combination thereof does not disclose, teach or suggest feature (ii)

From Figure 1 and paragraph [0021] of Tzeng, it can be seen that there appears to be 8 FE ports connected to the 10/100 transceiver 107 and 2 GE ports connected to the 10/100/1000 physical layer (PHY) 108. In other words, Tzeng teaches that a port only ever

operates as a single FE port or a single GE port. Clearly, Tzeng does not teach any port that is switchable between a first mode when the port operates as a single GE port and a second mode when the port operates as multiple FE ports. Therefore Tzeng does not disclose feature (ii).

Similarly, each port in Moran is only capable for operation as a single port i.e. either as a single FE port or a single GE port. Therefore, Moran does not disclose feature (ii).

A port configured to be switchable between the first and second modes as claimed in feature (ii) can be operated at much the same bandwidth (whether as a single GE port or as multiple FE ports) so its processing capacity can be used efficiently. Such a result is not predictable or expected by Tzeng, Moran or a valid combination thereof.

No Suggestion or Motivation to Combine Reference Teachings

For the avoidance of doubt, the applicant does not agree that there is any suggestion or motivation to combine the references. Applicant respectfully submits that while Tzeng is concerned with tying together multiple switch chips to achieve greater port density, Moran is concerned with bandwidth limitation for each port. Clearly, these references do not relate to efficiently using the bandwidth of all the hardware when operating in either FE or GE mode. Neither is there any motivation to combine these references.

Furthermore, the examiner has simply stated that "it would have been obvious to a person of ordinary skill in the art at the time of the invention to use separate send and receive memory modules in Tzeng's invention to reduce the possibility of undue delay, caused by long read/write cycles, by not having to search one large address pool to locate a packet or an

open slot for a received packet." Applicant respectfully submits that such a statement is an improper conclusory statement that is based on impermissible hindsight analysis. In any event, incorporating the separate transmit and receive storage modules, 29, 30 of Moran would render Tzeng inoperable and would not reduce delay.

Accordingly, applicant respectfully requests that the rejection under 35 U.S.C. §103(a) be withdrawn.

V. Rejection of Dependent Claims 9-16, 19-23 and 25-27 Under 35 U.S.C. § 103(a)

In the May 29, 2008 Office action, the examiner rejected dependent claims 9 – 11, 16, 19, 25 – 27 under 35 U.S.C. § 103(a) in view of Tzeng and further in view of Moran. In addition, the examiner rejected dependent claims 12 and 20 in view of Tzeng and Moran and further in view of Gentry, Jr. (US Pat 6,356,951), hereinafter referred to as "Gentry" and rejected dependent claims 13 – 15 and 21 – 23 in view of Tzeng, Moran and Gentry and further in view of Di Placido (US Pat 6,226,292).

As set forth above, the examiner's rejection of claims 8, 17 or 24 should be withdrawn. Therefore, because each of dependent claims 9 – 16, 19 – 23 and 25 – 27 depends from and incorporates all of the limitations of one of independent claims 8, 17 or 24, the examiner's rejection of dependent claims 9 – 16, 19 – 23 and 25 – 27 should also be withdrawn for at least the same reasons.

In addition, neither Gentry nor Di Placido discloses features (i) and (ii).

Gentry discloses that a communication packet may be received at NIC from network by a medium access control (MAC) module which performs low-level processing of the

packet such as reading the packet from the network, performing some error checking, detecting packet fragments, detecting over-sized packets, removing the layer one preamble, etc. (Column 7 lines 34 – 41) Clearly, Gentry does not disclose more than one MAC module and therefore certainly does not disclose receive and transmit modules which are configurable to interact with more than one MAC interface. Hence, Gentry does not disclose feature (i).

Neither does Gentry disclose any port that is switchable between a first mode of operating as a single GE port and a second mode of operating as multiple FE ports. Therefore, Gentry does not disclose feature (ii).

In Di Placido, the receive and transmit modules in a FE interface as disclosed in Figure 4 differs from the receive and transmit modules in a GE interface. For example, in Figure 4, the TX logic 34 includes a 128 byte first-in first out (FIFO) buffer (Column 5 lines 15 – 16) whereas in Figure 6, the TX logic 34 includes a 512 byte FIFO buffer (Column 5 lines 44 – 45). Clearly, the transmit module in a FE interface in Di Placido is not configurable to transmit GE packets. Therefore, Di Placido does not disclose feature (i).

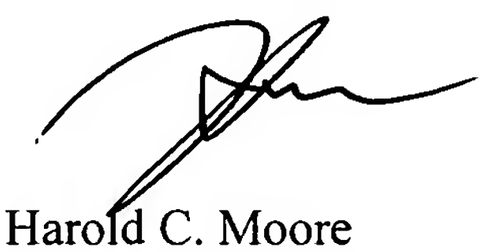
Di Placido discloses a switch including three 12-port Fast Ethernet network interfaces and one 3-port Gigabit Ethernet interface. Clearly, Di Placido does not disclose any port that is switchable between a first mode of operating as a single GE port and a second mode of operating as multiple FE ports i.e. Di Placido does not disclose feature (ii).

VI. Conclusion

For all of the foregoing reasons, it is respectfully submitted the applicant has made a patentable contribution to the art. Favorable reconsideration and allowance of this application is therefore respectfully requested.

In the event applicant has inadvertently overlooked the need for an extension of time or payment of an additional fee, the applicant conditionally petitions therefore, and authorizes any fee deficiency to be charged to deposit account 13-0014.

Respectfully submitted,



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